CLAIMS:

1. An apparatus for switching data frames comprising payload data arranged in accordance with a normal frame structure, the apparatus comprising a first switching component for switching high order data structures; a second switching component for switching low order data structures, the second switching component being subtended from said first switching component; and adaptation apparatus for adapting each data frame received by the apparatus for receiving data frames to a reference timing signal, wherein the adaptation apparatus is arranged to advance the payload data of a data frame with respect to its normal frame structure, and wherein the second switching component, during receipt of a data frame in respect of which the payload data has been so advanced, is arranged to generate an output data frame comprising said advanced payload data arranged in a normal frame structure so that said output frame is advanced with respect to the received data frame.

2. A switching apparatus as claimed in Claim 1, wherein data frames received by said switching apparatus further include fixed overhead, and the adaptation apparatus is arranged to advance the payload data of a data frame with respect to the fixed overhead of the data frame.

3. A switching apparatus as claimed in Claim 1, wherein said data frames further comprise one or more high order pointers, and the payload data comprises one or more low order data structures and one or more low order pointers the value of which indicate the position of the, or each, low order data structure, the value of the, or each, high

order pointer indicating the position of the, or each low order pointer, wherein the adaptation apparatus is arranged to advance the payload data by advancing the position of the, or each, low order pointer.

4. A switching apparatus as claimed in Claim 3, wherein the adaptation apparatus advances the, or each, low order pointer by adjusting the respective value of the, or each high order pointer.

5. A switching apparatus as claimed in Claim 3, wherein the, or each, low order pointer is normally positioned in a row of a data frame after the fixed overhead for said row, and wherein, after advancement, the, or each, low order pointer occurs before said fixed overhead.

6. A switching apparatus as claimed in Claim 5, wherein the, or each, low order pointer normally occurs in the first row of a data frame and wherein, after advancement, the, or each low order pointer occurs in a preceding data frame.

7. A switching apparatus as claimed in Claim 1, wherein the payload data is advanced by an amount corresponding to the delay incurred by a data frame in passing through the first switching component and the second switching component.

8. A switching apparatus as claimed in Claim 1, wherein the second switching component includes a plurality of data memories, the second switching component being arranged to, in respect of a received data frame, write successive blocks of received data in sequence to said

memories and, in order to create an output data frame, to read blocks of data in sequence from said memories, the respective sequences being such that while data is being written to one memory, data is being read from another memory, wherein the writing and reading of data to and from the memories is controlled by respective independent timing reference signals.

9. A switching apparatus as claimed in Claim 8, wherein the second switching component comprises a first and a second data memory, data blocks being written to and read from the first and second memories alternately.

10. A switching apparatus as claimed in Claim 8, wherein the second switching component comprises a write pointer generator for controlling the writing of data blocks to said memories, and a read pointer generator for controlling the reading of data blocks from said memories, wherein the operation of said write pointer generator is controlled by a first timing reference signal and the operation of said read pointer generator is controlled by a second timing reference signal, the first and second timing reference signals being independent of one another.

11. A switching apparatus as claimed in Claim 10, wherein the first and second timing reference signals are synchronized to the system reference timing signal.

12. A switching apparatus as claimed in Claim 11, wherein the second switching component includes one or more timing reference apparatus arranged to receive the system timing reference signal and to generate the first and second timing reference signals.

13. A switching apparatus as claimed in Claim 10, wherein the first timing reference signal is arranged to cause the write pointer generator to begin the writing of data to the memories at substantially the same time as the first block of payload data of a data frame is received by the second switching component.

14. A switching apparatus as claimed in Claim 10, wherein the write pointer generator is arranged to suspend the writing of data to the memories while fixed overhead data is received by the second switching component.

15. A switching apparatus as claimed in Claim 10, wherein the second switching component includes an overhead generator, the overhead generator being responsive to said second timing reference signal to generate overhead data, the read pointer generator being arranged to co-ordinate the reading of data blocks from the memories with the generation of overhead data in order to create an output data frame.

16. A switching apparatus as claimed in Claim 15, wherein the overhead generator is arranged to generate fixed overhead data denoting the beginning of an output data frame, the read pointer generator being arranged to cause a first payload data block to be read from one of said memories after said fixed overhead is generated.

17. A switching apparatus as claimed in Claim 1, arranged to switch data frames that are compliant with Synchronous Digital Hierarchy (SDH) and/or Synchronous Optical Network (SONET) standards.

18. A synchronous transmission apparatus comprising a switching apparatus as claimed in Claim 1.

19. A synchronous transmission system comprising a switching apparatus as claimed in Claim 1.

20. A synchronous transmission system as claimed in Claim 18, comprising a Synchronous Digital Hierarchy (SDH) and/or a Synchronous Optical Network (SONET) network.

21. In an apparatus for switching data frames comprising payload data arranged in accordance with a normal data frame structure, the apparatus comprising a first switching component for switching high order data structures; a second switching component for switching low order data structures, the second switching component being subtended from said first switching component; and adaptation apparatus for adapting each data frame received by the switching apparatus to a reference timing signal, a method of switching low order data structures, the method comprising: at the adaptation apparatus, advancing the payload data of a data frame with respect to its normal frame structure; and at the second switching component during receipt of a data frame in respect of which the payload data has been so advanced, generating an output data frame comprising said advanced payload data arranged in a normal frame structure so that said output frame is advanced with respect to the received data frame.

22. An apparatus for switching low order data structures, the apparatus being arranged to receive an input data frame comprising payload data and to generate an output

data frame comprising payload data, wherein the apparatus further includes a plurality of data memories and is arranged to, in respect of a received data frame, write successive blocks of received payload data in sequence to said memories and, in order to create an output data frame, to read blocks of payload data in sequence from said memories, the respective sequences being such that while data is being written to one memory, data is being read from another memory, wherein the writing and reading of data to and from the memories is controlled by respective independent timing reference signals.